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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,690	07/20/2006	Tadatomo Suga	YANE-0003-US1	6233

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EXAMINER	
PATEL, DEVANG R	
ART UNIT	PAPER NUMBER
1793	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/586,690	SUGA ET AL.	
	Examiner	Art Unit	
	DEVANG PATEL	1793	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) *21 and 26-49* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 22-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/29/07, 7/20/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 5-6, 8, 15, 17-19, and 22-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamauchi (**WO 2003001858 A1**). US 2004/0169020 is taken to be English-language equivalent of WO 2003001858 A1 and sections pointed out in the rejection below refer to the US publication.

a. **Regarding claim 1,** Yamauchi discloses a bonding method [fig. 1] for bonding objects to be bonded which have a bonding portion (4, 5) formed of a metal, wherein the bonding portions are gold/gold bonding [¶ 143], which inherently have a hardness of 200 Hv or less, are contacted with each other and pressed in a solid phase at room temperature [¶ 8-11] after treating the bonding portions with plasma [¶ 142, 12].

b. **As to claim 2,** Yamauchi discloses the bonding portions formed of gold.

c. **As to claim 5,** Yamauchi discloses atmospheric-pressure (i.e. low-pressure) plasma [¶ 146].

d. **As to claim 6,** Yamauchi discloses that least one of said objects to be bonded is a semiconductor; and that low-pressure plasma for cleaning is generated with electric field having alternating + and - directions generated by an alternating power supply 11/25/150 [figs. 1-4, 18].

e. **As to claim 8,** the oscillating power supply of Yamauchi is equivalent to a wave generating power supply and is capable of controlling a pulse width.

f. **As to claim 15,** Yamauchi discloses that the bonding portion is formed in the shape of a contour, said bonding portion is surface-activated with said energy wave, and thereafter, said objects to be bonded are bonded together in a solid phase at room temperature, so that space surrounded in said shape of contour by said bonding portions is formed between said bonding surfaces of said objects to be bonded to enclose a predetermined atmosphere in said space.

g. **As to claim 17,** Yamauchi discloses that bonding is performed in a vacuum, so that a vacuum atmosphere is enclosed in said space.

h. **As to claim 18,** Yamauchi discloses that after said surface activation of said bonding portion, a vacuum state of a low- pressure chamber is replaced with filling gas, and said objects to be bonded are bonded in said filling gas to enclose said filling gas atmosphere in said space [figs. 3, 5; ¶ 139, 147].

i. **As to claim 19**, Yamauchi discloses bonding in air [¶ 139].

j. **As to claim 22,** Yamauchi discloses the objects to be bonded are a chip, and a wafer [¶ 1, 3], being continuously bonded [figs. 3-4, 13]. It is well known in the art to mount a plurality of chips on a wafer.

k. **As to claim 23,** Yamauchi discloses that during the time when said chips are continuously bonded to said wafer, after a predetermined time has passed, said wafer is treated again with said energy wave [fig. 5 - while it is conveyed], and thereafter, bonding of said chips to said wafer is resumed [¶ 147].

l. **As to claims 24 & 25,** Yamauchi discloses semiconductor device.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. **Claims 3-4 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi as applied to claim 1 above, and in view of Gilleo et al. (US 5971253).

a. **As to claim 3,** Yamauchi discloses gold/gold bonding, however, it is unclear whether Yamauchi discloses forming a gold film on a surface of a base material (pad 5) having a hardness of 200 Hv or less, and after the objects are bonded together, the gold film is diffused into the base material. Gilleo et al. ("**Gilleo**") is drawn to microelectronic component mounting. Gilleo discloses [fig. 3] copper pads 56 [analogous to pads 5 of Yamauchi] on the substrate/chip 54, having a coating 58 [i.e. film] formed from gold or other diffusion bondable metal, and a diffusion bonding material 40 in conjunction with sheet 22 [figs. 8-9a; col. 7, lines 24-40]. The copper pads (base material) inherently have a hardness of 200 Hv or less. Diffusion bonding encompasses the gold film being diffused into the base material. Gilleo discloses that such bonding results in good connections even where the contacts of the chips and/or the pads of the substrate are slightly out of plane or of different heights [col. 7, lines 46-57]. It would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the bonding technique of Gilleo in the method of Yamauchi because doing so results in good connections even where the contacts of the chips and/or the pads of the substrate are slightly out of plane or of different heights.

b. **As to claim 4,** both Yamauchi and Gilleo disclose the object being a semiconductor. Gilleo discloses diffusing a gold film into the copper base material as explained in claim 3 above.

c. **As to claim 14,** Yamauchi and Gilleo as a whole discloses that bonding portion is treated with said energy wave, a metal electrode is provided at a position facing said bonding surface of at least one of said objects to be bonded, forming a metal film. Yamauchi also discloses that sputtering the bonding surfaces in room-temperature bonding method of silicon wafers is known [¶ 3]. It would have been obvious to form the metal film by sputtering since known technique of sputtering was recognized as part of ordinary capabilities of one skilled in the art.

4. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi as applied to claim 6 above, and in view of Linn et al. (US 5833758).

d. **As to claim 7,** it is unclear whether Yamauchi discloses RF plasma generating power supply. However, Linn et al. (**"Linn"**, drawn to method for cleaning semiconductor wafers) discloses two-step RF plasma cleaning process for wafers [col. 4, line 66 thru col. 3, line 10]. It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide RF plasma generation similar to Linn in the method of Yamauchi in order remove all contaminants from the surface and consequently improve bonding [abstract].

5. **Claims 9-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi as applied to claim 1 above, and in view of Linn et al. (US 5833758) and Usui et al. (US 2004/0140551).

e. **As to claim 9**, Yamauchi fails to disclose the bonding portion having a surface roughness. However, **Linn** discloses that argon plasma cleaning (similar

to Yamauchi) roughens the surface and enhances the solderability to the substrate by increasing the surface of the bonding layer [col. 3, lines 12-15]. It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide RF plasma generation similar to Linn in the method of Yamauchi in order remove all contaminants from the surface and consequently improve bonding [abstract]. Linn is silent about the roughness value. However, Usui et al. (**"Usui",** drawn to manufacturing semiconductor device) discloses surface processing a metal film to form a patterned interconnect line and to achieve surface roughness of 1 micron or less (i.e. greater than 120 nm), which effectively improves the high frequency performance [¶ 24; claim 14]. Thus, collective disclosures of Yamauchi, Linn and Usui teaches a bonding portion having the surface roughness value 120 nm or more, and providing so would have been obvious to a person of ordinary skill in the art at the time of the invention in order to increase the surface area and improve bonding strength [Linn] and device performance [Usui].

f. **As to claim 10,** Yamauchi discloses the bonding method including:

i. a head 7 [fig. 1] for holding one of the objects to be bonded;

ii. a stage 6 for holding the other object to be bonded; and

iii. a vertical drive mechanism for performing a position control with respect to at least one of said head and said stage in a direction substantially perpendicular to said bonding surface of said object to be bonded, and performing a pressing control [¶ 142],

iv. the vertical drive mechanism of Yamauchi is implicitly stopped at some point, when the bumps 4 and pads 5 are being bonded, thus it holds a constant height of the head 7 from said stage for a predetermined time.

6. **Claims 11-12 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi as applied to claims 1 and 19 above, respectively, and in view of Yagi et al. (US 5686353).

g. **As to claim 11-12,** Yamauchi does not disclose leveling the bonding portion. However, such is well known in the art. Yagi et al. ("**Yagi**") discloses leveling step to obtain uniform height of each of the bumps, and adapting the height of each of the bumps to corresponding height of each of the electrodes on the substrate [col. 5, line 33 thru col. 6, line 20]. It would have been obvious to a person of ordinary skill in the art at the time of the invention to perform leveling similar to Yagi in the method of Yamauchi in order to avoid the difficulties of non-uniformity and insufficient bonding strength [col. 3, lines 6-11].

h. **As to claim 20,** Yamauchi discloses electrically functioning device that employs the bonding portion as an electrode, bonding portion formed of gold, and cleaned with energy wave before bonding in air. However, it is unclear whether Yamauchi discloses adjusting optimum positions of the objects to be bonded while the device is caused to electrically function. **Yagi** discloses positioning the semiconductor device (i.e. chip) in relation to the substrate in a manner so as to transform the apex portion of each of the bumps and thus adapt height of each of the bumps to each of corresponding electrodes [col. 6, lines 4-

12]. Yagi further states that such provides extreme stability and accuracy, even if the electrodes have irregularity of thickness, or if the substrate has a warp or Yagi also discloses that the function test the electrical circuit is performed when the device is pressed against the substrate [col. 6, lines 22-28]. It would have been obvious to a person of ordinary skill in the art at the time of the invention to perform positioning step of Yagi in the method of Yamauchi because it provides extreme stability and accuracy, even if the electrodes have irregularity of thickness, or if the substrate has a warp or undulation [col. 6, lines 13-21].

7. **Claim 13** is rejected under 35 U.S.C. 103(a) as being obvious over Yamauchi (US 2004/0169020).

i. **As to claim 13,** Yamauchi discloses the bonding method including:

v. a chamber having a reduced pressure [¶ 145];

vi. Yamauchi discloses that the cleaning and bonding can be carried out in chambers different from each other [¶ 9]. The bonding surfaces of object 101 are not facing each other while being treated with energy wave 103 in cleaning chamber 102 [fig. 13]. It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide treat the bonding surfaces with energy wave while they are not facing each other because such is an art-recognized alternative.

vii. Yamauchi discloses moving one the objects (by conveying means 106- ¶ 154) so that the bonding surfaces 101a and 101b are facing each other in bonding chamber 105 [fig. 13].

viii. Yamauchi discloses that at least one of said objects to be bonded is moved in a direction substantially perpendicular to said bonding surface to contact said bonding portions with each other, and bond said objects to be bonded together in a solid phase.

8. **Claim 16** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi as applied to claim 15 above, and in view of Usui et al. (US 5686353).

m. **As to claim 16,** Yamauchi discloses bonding portion formed of gold but does not disclose the base material having hardness of 200 Hv or less, and a gold plating having a thickness of 1 micron or more. However, such arrangement is well known in the art as shown by Usui. **Usui** (directed to semiconductor device mounting) discloses a gold film 402 having a thickness of about 1-10 micron on a copper base material 400 [fig. 5a; ¶ 79]. The copper base material inherently has a hardness of 200 Hv or less. It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide the copper base and gold plating similar to Usui in the method of Yamauchi because doing so results in better adhesiveness and better plating [¶ 79], thus improving bonding strength.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 11/29/07, 7/20/06 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Conclusion

Claims 1-20 and 23-25 are rejected.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Yamauchi et al. (US 7279358), Platt et al. (US 6793829).

The rejections above rely on the references for all the teachings expressed in the text of the references and/or one of ordinary skill in the art would have reasonably understood from the texts. Only specific portions of the texts have been pointed out to emphasize certain aspects of the prior art, however, each reference as a whole should be reviewed in responding to the rejection, since other sections of the same reference and/or various combinations of the cited references may be relied on in future rejections in view of amendments.

Applicant is reminded to specifically point out the support for any amendments made to the disclosure. See 37 C.F.R. 1.121; 37 C.F.R. Part 41.37; and MPEP 714.02.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DEVANG PATEL whose telephone number is (571)270-3636. The examiner can normally be reached on Monday thru Thursday, 8:00 am to 5:30 pm, EST..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jessica Ward can be reached on 571-272-1223. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. P./
Examiner, Art Unit 1793

/Kiley Stoner/
Primary Examiner, Art Unit 1793